Reg. No. : ....

Name : ....

Fifth Semester B.Tech. Degree Examination, November 2011
(2008 Scheme)
08.505 – MICROPROCESSORS AND INTERFACING (R)

Time: 3 Hours　　　　　　　　　　　　　　　　　　　　　　Max. Marks: 100

PART – A

Answer **all** questions. **Each** question carries **4** marks.

1. Define Instruction cycle, Machine cycle and T-state. During which T-state the processor checks the status of Ready Signal.

2. If the memory chip size is 1024×4 bits, how many chips are required to make up 2k bytes of memory ? How many address lines are needed for addressing the memory.

3. Can an input port and an output port have the same port address in a 8085 based system ? Justify your answer In memory mapped I/O, can an I/O have the same address as a memory location ?

4. What is the resolution of a 13 bit D/A converter ? If the converter has a full scale output of 10 V, What is the size of each step ? What will be the maximum output voltage of this converter ?

5. In 8086 none of the registers is 20 bit. Explain with an example how 20 bit physical address is generated ? Can we have a segment of size less than 64 K ? Why ?

6. Illustrate how physical memory is organized in 8086 based system. Show the steps involved in accessing an odd addressed word from the memory ?

7. Explain the functions of the following signals :
   i) $\overline{\text{TEST}}$　　　　ii) READY　　　　iii) DT/$\overline{\text{R}}$　　　　iv) LOCK.

8. Explain Interrupt Vector Table (IVT) of 8086 system. What is address in the IVT for the interrupt of type 102 H ?

9. An 8255 (PPI) has a system base address of FFFOH. What are the system addresses for the three ports and the control register ? Write the mode set control word needed to initialize the 8255, as follows : Port A - hand-shake input, Port B - simple I/O output. Show the assembly language instructions you would use to send the control word to the 8255.

10. Explain the following terms in relation to the 8279 keyboard / display interface
   i) Two - key lockout   ii) N-key roll over
   iii) Right entry and left entry   iv) FIFO.

PART – B

Answer **one** full question from **each** Module. **Each** full question carries **20** marks.

Module – 1

11. a) Explain the pin diagram of 8085 (pin numbers not necessary) microprocessor by indicating the purpose of each signal.

   b) Discuss the addressing modes used in 8085 microprocessor.

OR

12. a) Design a memory system that contains 4K × 8 EPROM followed by 4K × 8 of RWM. The EPROM starts at 0000H and is implemented using 2K × 8 EPROM devices. Include the system memory map as part of the design. The RWM is implemented using 1K × 8 SRAM. Draw the logic diagram of the memory and its interface to the required signals from the 8085 system bus. Your diagram should contain details of all control signals $\left(\overline{CS}, \overline{OE} \text{ etc}\right)$ and decoder.

   b) Explain the principle of working of Digital to Analog converters.

Module – 2

13. a) With a neat diagram explain the architecture of 8086 microprocessor.

b) Write an assembly language program to move a string of N characters from a location pointed to by DS : SI to another location pointed to by ES : DI.

OR

14. a) Discuss the functional units in 8259 interrupt controller.

b) Write an assembly language program to sort a set of N 16 bit numbers in ascending orders.

Module – 3

15. a) Explain the organization of 8254 timer / counter.

b) The input frequency to the timer chip is 1.5 MHz write a program segment to generate a square wave of 1.5 KHz using counter O. The address of control register is CEH and the address of counter O is C_8H.

OR

16. a) Explain the idea of multiplexing a seven digit 7-segment display.

b) Explain the architecture of USART (8251).